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ABSTRACT OF THE DISCLOSURE

An apparatus comprising a phase lock loop (PLL) and a lock circuit. The PLL may be configured to multiply an input frequency in response to a lock signal. The lock circuit may be configured to generate the lock signal. The PLL may also be configured to select a reference frequency as (i) the input
5 frequency when in a first mode and (ii) a divided frequency of the input frequency when in a second mode.

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